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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/652,714	08/31/2000	Vishnu K. Agarwal	98-0616.09	3982

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EXAMINER

DIAZ, JOSE R

ART UNIT	PAPER NUMBER
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2815

DATE MAILED: 04/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/652,714

Applicant(s)

AGARWAL, VISHNU K.

Examiner

José R Díaz

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 24 March 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 37-39, 76-80 and 82-99 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 37-39, 76-80 and 82-99 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 21 6) ☐ Other: \_\_\_\_\_

### **DETAILED ACTION**

➤ The indicated allowability of claims 76-80 and 90-94 is withdrawn in view of the newly discovered reference(s) to Hintermaier et al. (US Patent No. 6,100,187). Rejections based on the newly cited reference(s) follow.

#### ***Continued Examination Under 37 CFR 1.114***

➤ A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 24, 2003 has been entered.

#### ***Claim Rejections - 35 USC § 102***

➤ The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

➤ Claims 37-38, 82, 84, 86-88, 95-96 and 98 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee (US Pat. No. 5,846,859), which was cited in paper No. 18.

- Regarding claims 37, 82, 84, 86-87 and 95-96, Lee teaches a method of forming a semiconductor device comprising the steps of: depositing a first conductive (18) (see Fig. 1), incorporating an oxygen-free material directly into said first conductive, the oxygen-free material being selected from a group consisting of phosphine and methylsilane (see col. 4, lines 64-67), depositing a second conductive layer (24, 26, 28, 30) (see Fig. 1), exposing the second conductive layer (24, 26, 28, 30) to a thermal process, wherein said exposing step comprises: depositing an insulator (32) over the second conductive layer and flowing said insulator (see Figs. 1 and 2F, and col. 5, lines 63-65).
- Regarding claims 38, 88, and 98, Lee teaches that said step of depositing a first conductive layer comprises depositing a plug (18) (see Fig. 1).

### ***Claim Rejections - 35 USC § 103***

➤ The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

➤ Claims 37, 82, 86-87 and 95-96 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (US 2001/0001501 A1) in view of Applicant's Specification.

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- Regarding claims 37, 82, 86-87 and 95-96, Lee et al. teach teaches a method of forming a semiconductor device comprising the steps of: depositing a first conductive (21) (see Fig. 1B), incorporating an oxygen-free material directly into said first conductive, the oxygen-free material being selected from a group consisting of phosphine and methylsilane (see paragraph [0031] on pages 3-4), depositing a second conductive layer (22, 23, 24) (see Fig. 1B). However, the reference Lee et al. is silent with regards to the further step of exposing the second conductive layer to a thermal process, wherein said exposing step comprises: depositing an insulator over the second conductive layer and flowing said insulator. Applicant acknowledges that is well known in the art to further perform a thermal process to form a BPSG layer (34) over the second conductive layer of the capacitor (see [page 6, lines 5-9]). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to modify Lee et al. to include the step of further performing a thermal process, which includes the further steps of: depositing an insulator over the second conductive layer and flowing said insulator. The ordinary artisan would have been motivated to modify Lee et al.. in the manner described above for at least the purpose of electrically isolating one level of conductor from another in multilevel-interconnect system.

➤ Claims 37, 38, 76-77, 79, 82, 84, 86-88, 90-91, 93, 95-96 and 98 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park et al. (US Pat. No.5,723,384)

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in view of Hintermaier et al. (US Patent No. 6,100,187), and further in view of Applicant's Specification.

- Regarding claims 37-38, 76-77, 79, 82, 84, 86-88, 90-91, 93, 95-96 and 98, Park et al. teach a method for fabricating a capacitor (see Fig. 15) comprising the steps of: providing the first conductive plug (35) (see Fig. 11), providing a conductive barrier (39) comprised of  $WN_x$  (see Fig. 15) and forming the second conductive layer (see col. 4, lines 32-33). However, Park et al. fails to teach the limitation of treating the surface of the barrier surface with a material selected from the group of phosphine and methylsilane before to form the second conductive layer. Hintermaier et al. teach a method in which a barrier layer of a capacitor is treated with  $PH_3$  (see col. 4, lines 33-41). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to modify Park et al. to include the step of treating the surface of the conductive barrier layer with phosphine prior to the step of forming the second conductive layer. The ordinary artisan would have been motivated to modify Park et al. in the manner described above for at least the purpose of preventing the oxidation of the contact plug.

A further difference between the prior art and the present invention is the further step of exposing the second conductive layer to a thermal process, wherein said exposing step comprises: depositing an insulator over the second conductive layer and flowing said insulator. However, Applicant acknowledges that is well known in the art to further perform a thermal process to form a BPSG

layer (34) over the second conductive layer of the capacitor (see [page 6, lines 5-9). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to further modify Park et al. to include the step of further performing a thermal process, which includes the further steps of: depositing an insulator over the second conductive layer and flowing said insulator. The ordinary artisan would have been motivated to further modify Park et al. in the manner described above for at least the purpose of electrically isolating one level of conductor from another in multilevel-interconnect system.

➤ Claims 39, 78, 83, 85, 89, 92, 94, 97 and 99 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park et al. (US Pat. No.5,723,384) in view of Hintermaier et al. (US Patent No. 6,100,187) and Applicant's Specification, and further in view of Mark et al. (US Pat. No. 6,309,713 B1).

- Regarding claims 39, 78, 80, 83, 85, 89, 92, 94, 97 and 99, a further different between the present invention and the prior art is the material, which was used to form the second conductive layer or upper electrode. Mark et al. ('713) teach that is well known in the art to use copper as the second conductive layer in a capacitor structure comprised of a  $WN_x$  barrier layer (see col. 4, lines 62-67 and col.5, lines 13-15). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to further modify Park et al. to include a second conductive layer formed of copper. The ordinary artisan would have been motivated to further modify Park et al. in the manner described

above for at least the purpose of providing electrical contact to other semiconductor devices.

### ***Response to Arguments***

➤ Applicant's arguments with respect to claims 37-39, 76-80, 82-99 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

➤ The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references are related to the present invention: Argarwal (US Pat. Nos. 6,472,264 B1 and 6,468,854 B1).

### ***Correspondence***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R Díaz whose telephone number is (703) 308-6078. The examiner can normally be reached on 9:00-5:00 Monday, Tuesday, Thursday and Friday.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 746-3891 for After Final communications.



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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JRD  
April 22, 2003



EDDIE LEE  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800